What is claimed is:

1. A flash memory device comprising:

a memory array having erasable blocks of memory cells, each block of memory cells being arranged in a row and column configuration, wherein each column of memory cells is couplable to an associated bit line;

control circuitry to control memory operations to the memory array;

a verify sense amplifier to verify a program state of the memory cells, the verify sense amplifier is coupled to a first location of the bit lines;

a read sense amplifier to read a program state of the memory cells, the read sense amplifier is coupled to a second location of the bit lines; and

a switch to selectively couple either the verify sense amplifier or the read sense amplifier to an output circuit.

2. The flash memory device of claim 1 wherein the flash memory is a synchronous flash memory.

3. The flash memory device of claim 1 wherein the verify sense amplifier and the read sense amplifier have adjustable sensitivity.

4. The flash memory device of claim 1 wherein the read sense amplifier comprises transistors with a gate oxide of approximately 200 Å and the read sense amplifier comprises transistors with a gate oxide of approximately 70 Å.

5. A flash memory comprising:

an array of memory cells;

a first read path having a first read circuit;

a second read path having a second read circuit; and

switch circuitry to select the first or second read circuits and couple to external data connections.

6. The flash memory of claim 5 wherein the second read circuit comprises a verify circuit used during erase and program operations.

7. The flash memory of claim 5 wherein the first read circuit comprises a read circuit used during read operations.

8. The flash memory of claim 5 wherein the second read circuit comprises an adjustable verify sense amplifier circuit.

9. The flash memory of claim 5 wherein the first read circuit comprises an adjustable read sense amplifier circuit.

10. The flash memory of claim 5 wherein the switch circuitry is activated during a test operation to allow calibration testing between the first and second read circuits.

11. A system comprising:

a memory test circuit; and

flash memory coupled to the memory test circuit comprising,

an array of memory cells,

a first read path having a first read circuit,

a second read path having a second read circuit, and

switch circuitry to select the first or second read circuits and couple to the memory test circuit via external data connections.

12. The system of claim 11 wherein the memory test circuit determines offset between the first and second read circuits.

13. The system of claim 12 wherein the flash memory comprises a control circuit to adjust either the first or second read circuits in response to the memory test circuit.

14. A method of calibrating a non-volatile memory comprising:

reading a data state of a plurality of memory cells with a first sense amplifier;

reading the data state of the plurality of memory cells with a second sense amplifier;

comparing outputs of the first and second sense amplifiers to determine offsets between the first and second sense amplifiers; and

adjusting either the first or second sense amplifier to calibrate the first and second sense amplifiers.

15. The method of claim 14 wherein the 5 wherein the first sense amplifier is used during erase and program operations.

16. The method of claim 14 wherein the second sense amplifier is used during read operations.

17. The method of claim 14 wherein the non-volatile memory is a flash memory.

18. The method of claim 14 wherein comparing the outputs of the first and second sense amplifiers is performed by an external test circuit.

19. The method of claim 14 wherein adjusting either the first or second sense amplifier comprises changing a voltage sensitivity of the sense amplifier.

20. A method of calibrating a flash memory comprising:

storing a test pattern in the flash memory;

reading the test pattern with a first read circuit;

reading the test pattern with a second read circuit;

outputting the read test pattern from the first and second read circuit to an external connection;

using an external tester, determining if an offset exits between the first and second read circuits; and

adjusting either the first or second read circuit if an offset id determined.